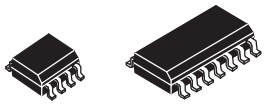




# MULTIPOINT-LVDS LINE DRIVER AND RECEIVER

## FEATURES

- **Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates(1) Up to 200 Mbps**
- **Type-1 Receivers Incorporate 25 mV of Hysteresis**
- **Type-2 Receivers Provide an Offset (100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions**
- **Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**
- **-1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise**
- **Bus Pins High Impedance When Disabled or $V_{CC}$ ≤ 1.5 V**
- **100-Mbps Devices Available (SN65MLVD200A, 202A, 204A, 205A)**
- **M-LVDS Bus Power Up/Down Glitch Free**

The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

## APPLICATIONS

- **Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485**
- **Backplane or Cabled Multipoint Data and Clock Transmission**
- **Cellular Base Stations**
- **Central-Office Switches**
- **Network Switches and Routers**

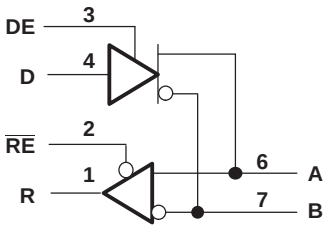
## DESCRIPTION

The SN65MLVD201, 203, 206, and 207 are multipoint-low-voltage differential (M-LVDS) line drivers and receivers, which are optimized to operate at signaling rates up to 200 Mbps. All parts comply with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899. These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts, with added features to address multipoint applications. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

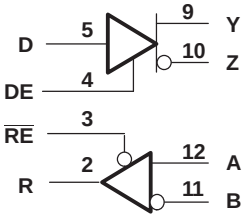
These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of -1 V to 3.4 V. The Type-1 receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. Type-2 receivers include an offset threshold to provide a known output state under open-circuit, idle-bus, and other faults conditions. The devices are characterized for operation from –40°C to 85°C.

## LOGIC DIAGRAM (POSITIVE LOGIC)

**SN65MLVD201, SN65MLVD206**




**SN65MLVD203, SN65MLVD207**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| PART NUMBER(1) | FOOTPRINT | RECEIVER TYPE | PACKAGE MARKING |
|---|---|---|---|
| SN65MLVD201D | SN75176 | Type 1 | MF201 |
| SM65MLVD203D | SN75ALS180 | Type 1 | MLVD203 |
| SN65MLVD206D | SN75176 | Type 2 | MF206 |
| SM65MLVD207D | SN75ALS180 | Type 2 | MLVD207 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## PACKAGE DISSIPATION RATINGS

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 85°C$ POWER RATING |
|---|---|---|---|
| D(8) | 725 mW | 5.8 mW/°C | 377 mW |
| D(14) | 950 mW | 7.6 mW/°C | 494 mw |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | | VALUE / UNIT |
|---|---|---|---|
| Supply voltage range(2), $V_{CC}$ | | | –0.5 V to 4 V |
| Input voltage range | D, DE, $\overline{RE}$ | | –0.5 V to 4 V |
| | A, B (201, 206) | | –1.8 V to 4 V |
| | A, B (203, 207) | | –4 V to 6 V |
| Output voltage range | R | | –0.3 V to 4 V |
| | Y, Z, A, or B | | –1.8 V to 4 V |
| Electrostatic discharge | Human Body Model(3) | A, B, Y, and Z | ±8 kV |
| | | All pins | ±2 kV |
| | Charged-Device Model(4) | All pins | ±1500 V |
| Continuous power dissipation | | | See Dissipation Rating Table |
| Storage temperature range | | | –65°C to 150°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | GND | | 0.8 | V |
| | Voltage at any bus terminal $V_A$, $V_B$, $V_Y$ or $V_Z$ | –1.4 | | 3.8 | V |
| $\lvert V_{ID} \rvert$ | Magnitude of differential input voltage | 0.05 | | $V_{CC}$ | V |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

## DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}$ Supply current | Driver only | $\overline{RE}$ and DE at $V_{CC}$, $R_L$ = 50 Ω, All others open | | 13 | 22 | mA |
| | Both disabled | $\overline{RE}$ at $V_{CC}$, DE at 0 V, $R_L$ = No Load, All others open | | 1 | 4 | |
| | Both enabled | $\overline{RE}$ at 0 V, DE at $V_{CC}$, $R_L$ = 50 Ω, All others open | | 16 | 24 | |
| | Receiver only | $\overline{RE}$ at 0 V, DE at 0 V, $R_L$ = 50 Ω, All others open | | 4 | 13 | |

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN(1) | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\|V_{AB}\|$ or $\|V_{YZ}\|$ | Differential output voltage magnitude | See Figure 2 | 480 | | 650 | mV |
| $\Delta\|V_{AB}\|$ or $\Delta\|V_{YZ}\|$ | Change in differential output voltage magnitude between logic states | | –50 | | 50 | mV |
| $V_{OS(SS)}$ | Steady-state common-mode output voltage | See Figure 3 | 0.8 | | 1.2 | V |
| $\Delta V_{OS(SS)}$ | Change in steady-state common-mode output voltage between logic states | | –50 | | 50 | mV |
| $V_{OS(PP)}$ | Peak-to-peak common-mode output voltage | | | | 150 | mV |
| $V_{Y(OC)}$ or $V_{A(OC)}$ | Maximum steady-state open-circuit output voltage | See Figure 7 | 0 | | 2.4 | V |
| $V_{Z(OC)}$ or $V_{B(OC)}$ | Maximum steady-state open-circuit output voltage | | 0 | | 2.4 | V |
| $V_{P(H)}$ | Voltage overshoot, low-to-high level output | See Figure 5 | | | 1.2 $V_{SS}$ | V |
| $V_{P(L)}$ | Voltage overshoot, high-to-low level output | | –0.2 $V_{SS}$ | | | V |
| $I_{IH}$ | High-level input current (D, DE) | $V_{IH}$ = 2 V | 0 | | 10 | µA |
| $I_{IL}$ | Low-level input current (D, DE) | $V_{IL}$ = 0.8 V | 0 | | 10 | µA |
| $\|I_{OS}\|$ | Differential short-circuit output current magnitude | See Figure 4 | | | 24 | mA |
| $I_{OZ}$ | High-impedance state output current (driver only) | –1.4 V ≤ $V_Y$ or $V_Z$ ≤ 3.8 V, Other output = 1.2 V | –15 | | 10 | µA |
| $I_{O(OFF)}$ | Power-off output current | –1.4 V ≤ $V_Y$ or $V_Z$ ≤ 3.8 V, Other output = 1.2 V, 0 V ≤ $V_{CC}$ ≤ 1.5 V | –10 | | 10 | µA |
| $C_Y$ or $C_Z$ | Output capacitance | $V_I$ = 0.4 sin(30E6πt) + 0.5 V, (3) Other input at 1.2 V, Driver disabled | | 3 | | pF |
| $C_{YZ}$ | Differential output capacitance | $V_{AB}$ = 0.4 sin(30E6πt) V, (3) Driver disabled | | | 2.5 | pF |
| $C_{Y/Z}$ | Output capacitance balance, ($C_Y/C_Z$) | | 0.99 | | 1.01 | |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.
(3) HP4194A impedance analyzer (or equivalent)

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input voltage threshold | Type 1 | See Figure 9 and Table 1 and Table 2 | | | 50 | mV |
| | | Type 2 | | | | 150 | |
| $V_{IT-}$ | Negative-going differential input voltage threshold | Type 1 | | –50 | | | mV |
| | | Type 2 | | 50 | | | |
| $V_{HYS}$ | Differential input voltage hysteresis, ($V_{IT+} – V_{IT}$) | Type 1 | | | 25 | | mV |
| | | Type 2 | | | 0 | | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –8 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current ($\overline{RE}$) | | $V_{IH}$ = 2 V | –10 | | 0 | µA |
| $I_{IL}$ | Low-level input current ($\overline{RE}$) | | $V_{IL}$ = 0.8 V | –10 | | 0 | µA |
| $I_{OZ}$ | High-impedance output current | | $V_O$ = 0 V or 3.6 V | –10 | | 15 | µA |
| $C_A$ or $C_B$ | Input capacitance | | $V_I$ = 0.4 sin(30E6πt) + 0.5 V,(2) Other input at 1.2 V | | 3 | | pF |
| $C_{AB}$ | Differential input capacitance | | $V_{AB}$ = 0.4 sin(30E6πt) V(2) | | | 2.5 | pF |
| $C_{A/B}$ | Input capacitance balance, ($C_A/C_B$) | | | 0.99 | | 1.01 | |

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) HP4194A impedance analyzer (or equivalent)

## BUS INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_A$ | Receiver or transceiver with driver disabled input current | $V_A$ = 3.8 V, | $V_B$ = 1.2 V, | | 0 | | 32 | µA |
| | | $V_A$ = 0 V or 2.4 V, | $V_B$ = 1.2 V | | –20 | | 20 | |
| | | $V_A$ = –1.4 V, | $V_B$ = 1.2 V | | –32 | | 0 | |
| $I_B$ | Receiver or transceiver with driver disabled input current | $V_B$ = 3.8 V, | $V_A$ = 1.2 V | | 0 | | 32 | µA |
| | | $V_B$ = 0 V or 2.4 V, | $V_A$ = 1.2 V | | –20 | | 20 | |
| | | $V_B$ = –1.4 V, | $V_A$ = 1.2 V | | –32 | | 0 | |
| $I_{AB}$ | Receiver or transceiver with driver disabled differential input current ($I_A - I_B$) | $V_A = V_B$, | 1.4 ≤ $V_A$ ≤ 3.8 V | | -4 | | 4 | µA |
| $I_{A(OFF)}$ | Receiver or transceiver power-off input current | $V_A$ = 3.8 V, | $V_B$ = 1.2 V, | 0 V ≤ $V_{CC}$ ≤ 1.5 V | 0 | | 32 | µA |
| | | $V_A$ = 0 V or 2.4 V, | $V_B$ = 1.2 V, | 0 V ≤ $V_{CC}$ ≤ 1.5 V | –20 | | 20 | |
| | | $V_A$ = –1.4 V, | $V_B$= 1.2 V, | 0 V ≤ $V_{CC}$ ≤ 1.5 V | –32 | | 0 | |
| $I_{B(OFF)}$ | Receiver or transceiver power-off input current | $V_B$ = 3.8 V, | $V_A$ = 1.2 V, | 0 V ≤ $V_{CC}$ ≤ 1.5 V | 0 | | 32 | µA |
| | | $V_B$ = 0 V or 2.4 V, | $V_A$ = 1.2 V, | 0 V ≤ $V_{CC}$ ≤ 1.5 V | –20 | | 20 | |
| | | $V_B$ = –1.4 V, | $V_A$ = 1.2 V, | 0 V ≤ $V_{CC}$ ≤ 1.5 V | –32 | | 0 | |
| $I_{AB(OFF)}$ | Receiver input or transceiver power-off differential input current ($I_A - I_B$) | $V_A = V_B$, 0 V ≤ $V_{CC}$ ≤ 1.5 V, –1.4 ≤ $V_A$ ≤ 3.8 V | | | –4 | | 4 | µA |
| $C_A$ | Transceiver with driver disabled input capacitance | $V_A$ = 0.4 sin (30E6πt) + 0.5V(2), | $V_B$ = 1.2 V | | | 5 | | pF |
| $C_B$ | Transceiver with driver disabled input capacitance | $V_B$ = 0.4 sin (30E6πt) + 0.5 V(2), | $V_A$ = 1.2 V | | | 5 | | pF |
| $C_{AB}$ | Transceiver with driver disabled differential input capacitance | $V_{AB}$ = 0.4 sin (30E6πt)V(2) | | | | | 3 | pF |
| $C_{A/B}$ | Transceiver with driver disabled input capacitance balance, ($C_A/C_B$) | | | | 0.99 | | 1.01 | |

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) HP4194A impedance analyzer (or equivalent)

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 5 | 1 | 1.5 | 2.4 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 1 | 1.5 | 2.4 | ns |
| $t_r$ | Differential output signal rise time | | 1 | | 1.6 | ns |
| $t_f$ | Differential output signal fall time | | 1 | | 1.6 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} - t_{PLH}\|$) | | | 0 | 100 | ps |
| $t_{sk(pp)}$ | Part-to-part skew(2) | | | | 1 | ns |
| $t_{jit(per)}$ | Period jitter, rms (1 standard deviation)(3) | 100 MHz clock input(4) | | 2 | 3 | ps |
| $t_{jit(pp)}$ | Peak-to-peak jitter(3) (5) | 200 Mbps $2^{15}$–1 PRBS input(6) | | 30 | 130 | ps |
| $t_{PHZ}$ | Disable time, high-level-to-high-impedance output | See Figure 6 | | | 7 | ns |
| $t_{PLZ}$ | Disable time, low-level-to-high-impedance output | | | | 7 | ns |
| $t_{PZH}$ | Enable time, high-impedance-to-high-level output | | | | 7 | ns |
| $t_{PZL}$ | Enable time, high-impedance-to-low-level output | | | | 7 | ns |

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(4) $t_r = t_f$ = 0.5 ns (10% to 90%), measured over 30 k samples.
(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).
(6) $t_r = t_f$ = 0.5 ns (10% to 90%), measured over 100 k samples.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pLH}$ | Propagation delay time, low-to-high-level output | | $C_L$ = 15 pF, See Figure 10 | 2 | 4 | 6 | ns |
| $t_{pHL}$ | Propagation delay time, high-to-low-level output | | | 2 | 4 | 6 | ns |
| $t_r$ | Output signal rise time | | | 1 | | 2.3 | ns |
| $t_f$ | Output signal fall time | | | 1 | | 2.3 | ns |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$) | Type 1 | | | 100 | 300 | ps |
| | | Type 2 | | | 300 | 500 | ps |
| $t_{sk(pp)}$ | Part-to-part skew(2) | | | | | 1 | ns |
| $t_{jit(per)}$ | Period jitter, rms (1 standard deviation) (3) | | 100 MHz clock input(4) | | 4 | 7 | ps |
| $t_{jit(pp)}$ | Peak-to-peak jitter(3)(5) | Type 1 | 200 Mbps $2^{15}$–1 PRBS input(6) | | 300 | 700 | ps |
| | | Type 2 | | | 450 | 800 | ps |
| $t_{pHZ}$ | Disable time, high-level-to-high-impedance output | | See Figure 11 | | | 10 | ns |
| $t_{pLZ}$ | Disable time, low-level-to-high-impedance output | | | | | 10 | ns |
| $t_{pZH}$ | Enable time, high-impedance-to-high-level output | | | | | 15 | ns |
| $t_{pZL}$ | Enable time, high-impedance-to-low-level output | | | | | 15 | ns |

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(4) $V_{ID}$ = 200 $mV_{pp}$ (LVD201, 203), $V_{ID}$ = 400 $mV_{pp}$ (LVD206, 207), $V_{cm}$ = 1 V, $t_r$ = $t_f$ = 0.5 ns (10% to 90%), measured over 30 k samples.
(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).
(6) $V_{ID}$ = 200 $mV_{pp}$ (LVD201, 203), $V_{ID}$ = 400 $mV_{pp}$ (LVD206, 207), $V_{cm}$ = 1 V, $t_r$ = $t_f$ = 0.5 ns (10% to 90%), measured over 100 k samples.

## PARAMETER MEASUREMENT INFORMATION

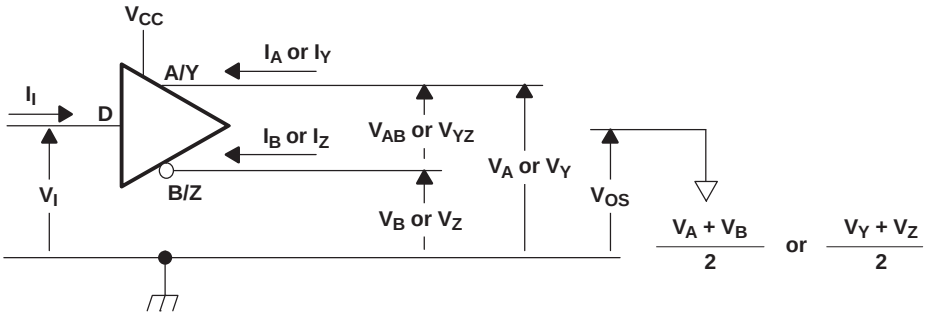
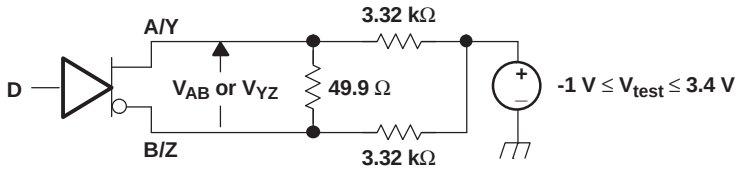
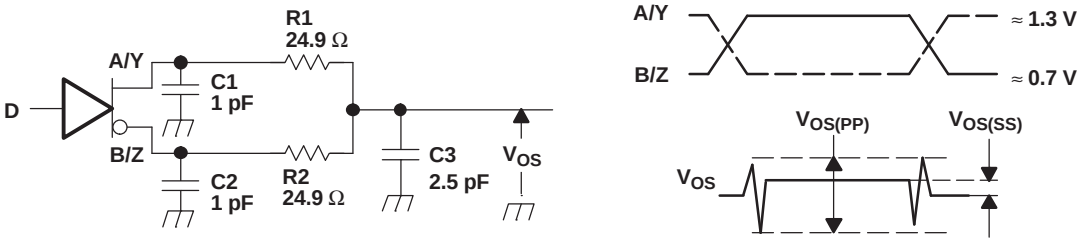



**Figure 1. Driver Voltage and Current Definitions**




A. All resistors are 1% tolerance.

**Figure 2. Differential Output Voltage Test Circuit**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$≤ 1 ns, pulse frequency = 500 kHz, duty cycle = 50 ± 5%.

B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.

C. R1 and R2 are metal film, surface mount, 1%, and located within 2 cm of the D.U.T.

D. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**

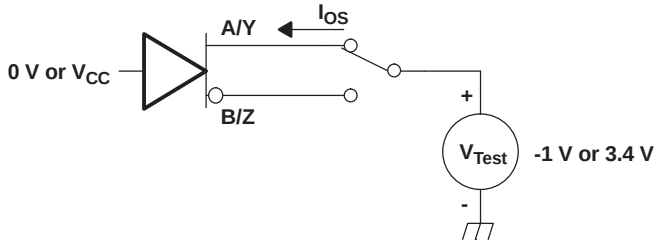
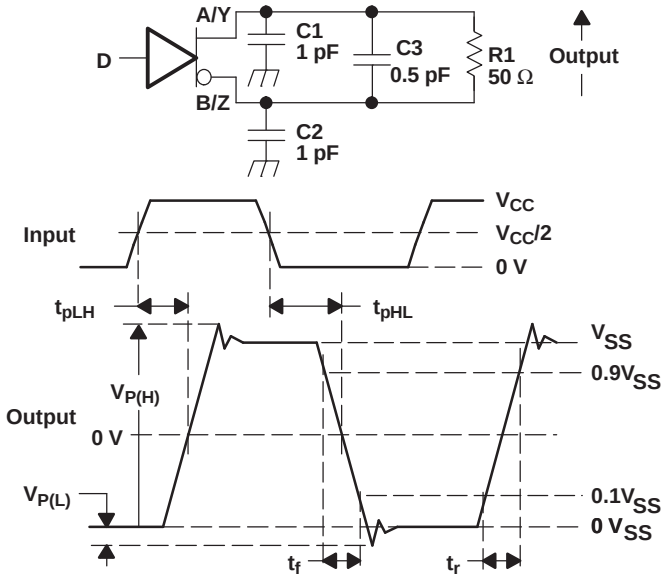



**Figure 4. Driver Short-Circuit Test Circuit**

## PARAMETER MEASUREMENT INFORMATION (continued)



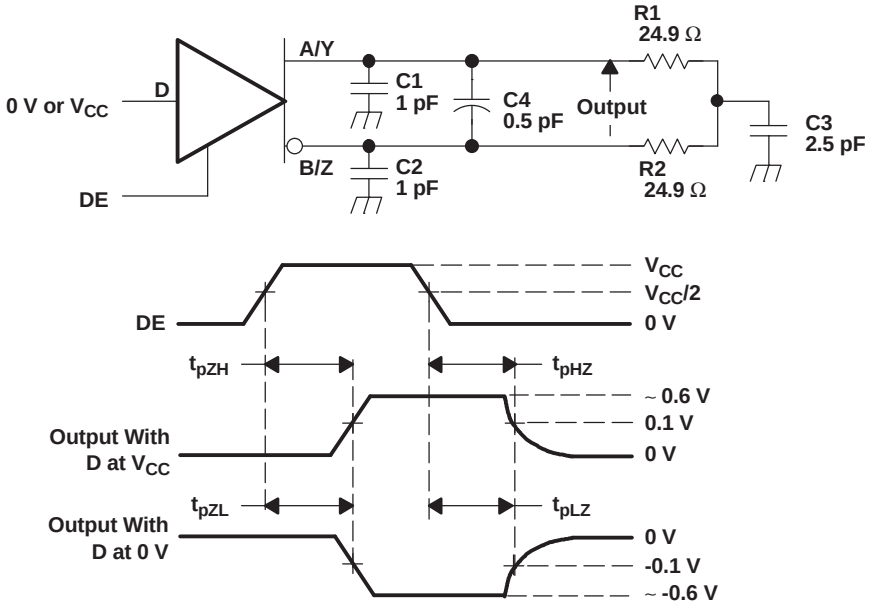

A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$≤ 1 ns, frequency = 500 kHz, duty cycle = 50 5%.

B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.

C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

**Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$≤ 1 ns, frequency = 500 kHz, duty cycle = 50 5%.

B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.

C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

**Figure 6. Driver Enable and Disable Time Circuit and Definitions**

## PARAMETER MEASUREMENT INFORMATION (continued)

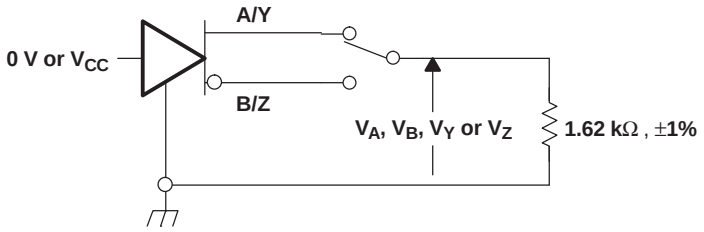
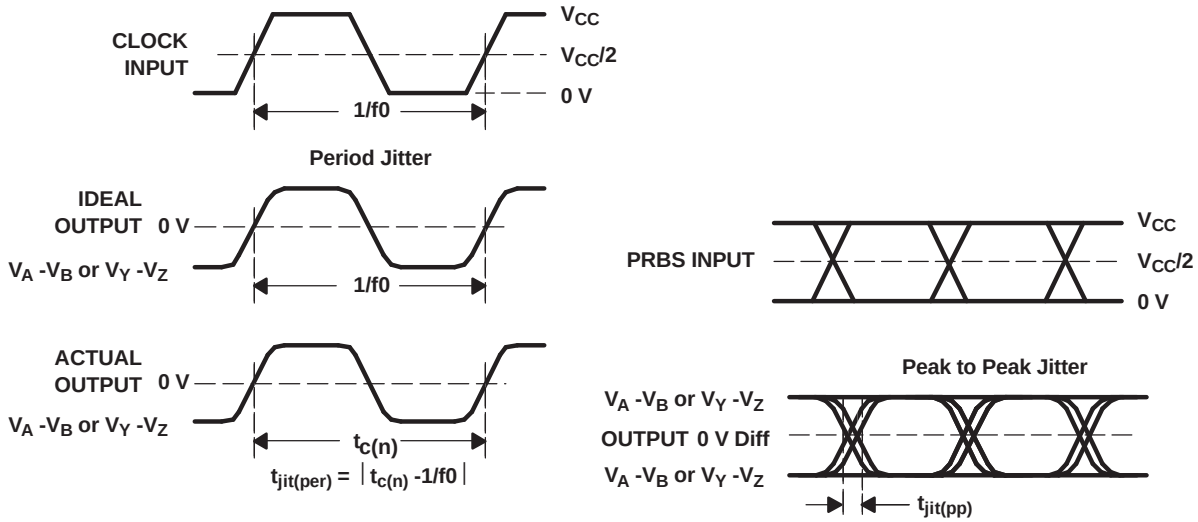



**Figure 7. Maximum Steady State Output Voltage**




A. All input pulses are supplied by an Agilent 8304A Stimulus System.

B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software

C. Period jitter is measured using a 100 MHz 50 1% duty cycle clock input.

D. Peak-to-peak jitter is measured using a 200Mbps $2^{15}$-1 PRBS input.

**Figure 8. Driver Jitter Measurement Waveforms**

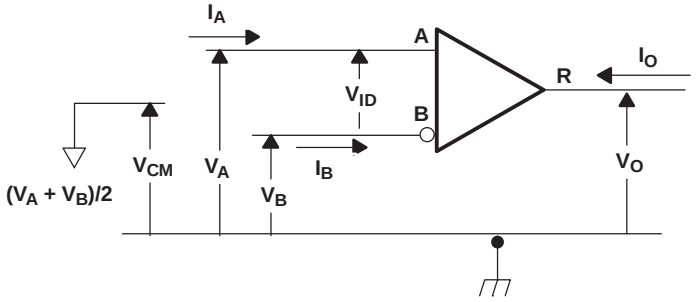



**Figure 9. Receiver Voltage and Current Definitions**

**Table 1. Type-1 Receiver Input Threshold Test Voltages**

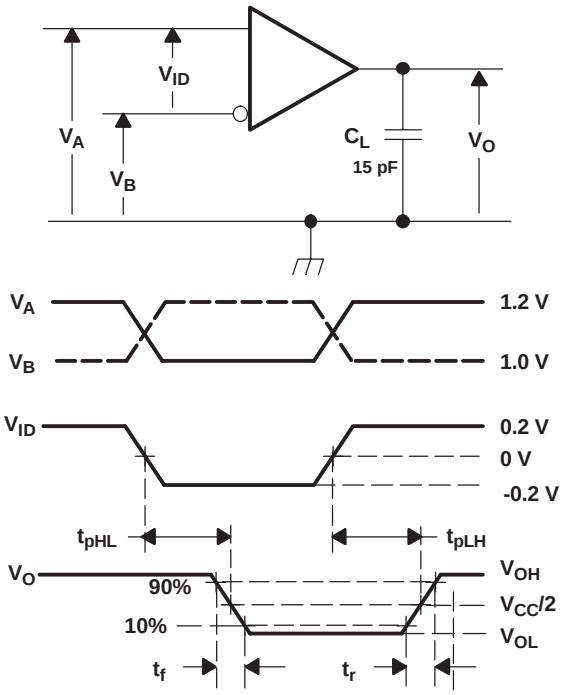
| APPLIED VOLTAGES | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE | RECEIVER OUTPUT(1) |
|---|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ | |
| 2.400 | 0.000 | 2.400 | 1.200 | H |
| 0.000 | 2.400 | –2.400 | 1.200 | L |
| 3.800 | 3.750 | 0.050 | 3.775 | H |
| 3.750 | 3.800 | –0.050 | 3.775 | L |
| –1.350 | –1.400 | 0.050 | –1.375 | H |
| –1.400 | –1.350 | –0.050 | –1.375 | L |

(1) H = high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)

**Table 2. Type-2 Receiver Input Threshold Test Voltages**

| APPLIED VOLTAGES | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE | RECEIVER OUTPUT(1) |
|---|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ | |
| 2.400 | 0.000 | 2.400 | 1.200 | H |
| 0.000 | 2.400 | –2.400 | 1.200 | L |
| 3.800 | 3.650 | 0.150 | 3.725 | H |
| 3.800 | 3.750 | 0.050 | 3.775 | L |
| –1.250 | –1.400 | 0.150 | –1.325 | H |
| –1.350 | –1.400 | 0.050 | –1.375 | L |

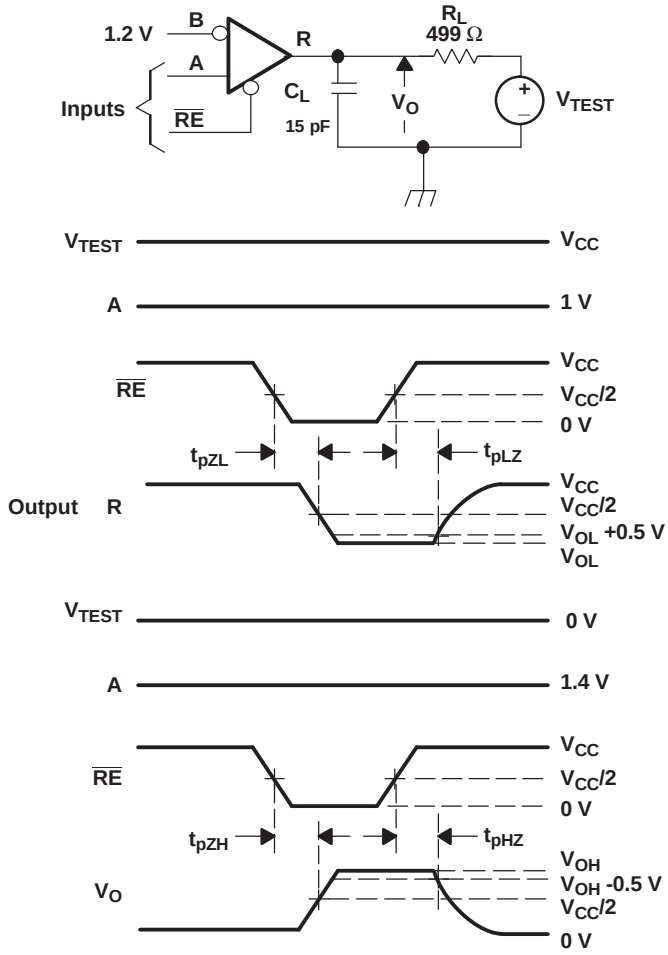
(1) H = high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$≤ 1 ns, frequency = 50 MHz, duty cycle = 50 5%. $C_L$ is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

B. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 10. Receiver Timing Test Circuit and Waveforms**



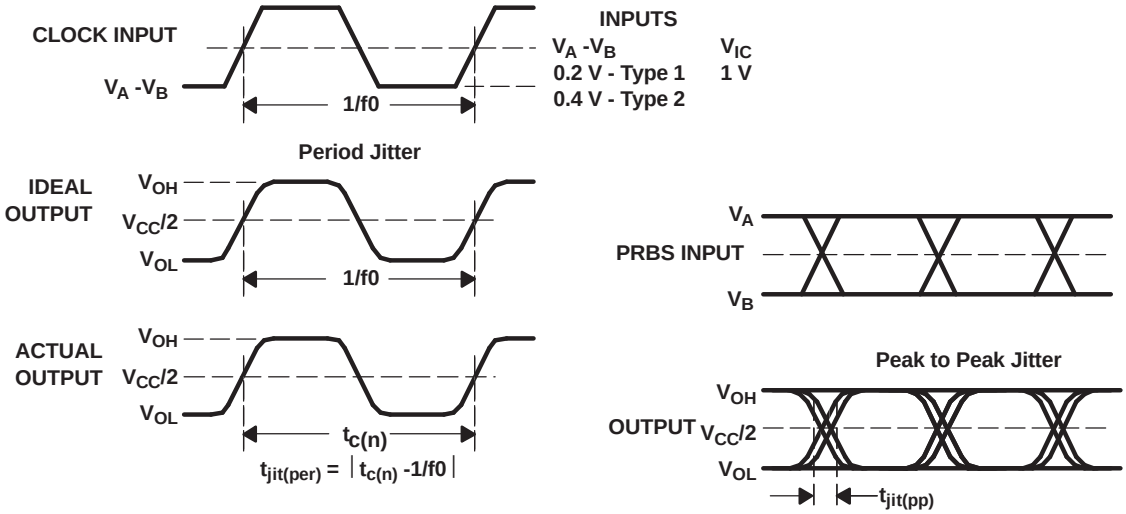

A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$≤ 1 ns, frequency = 500 kHz, duty cycle = 50 5%.

B. $R_L$ is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.

C. $R_L$ is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.

D. $C_L$ is the instrumentation and fixture capacitance within 2 cm of the DUT and 20%.

**Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms**




A. All input pulses are supplied by an Agilent 8304A Stimulus System.

B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software

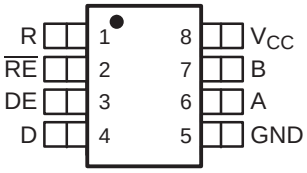
C. Period jitter is measured using a 100 MHz 50 1% duty cycle clock input.

D. Peak-to-peak jitter is measured using a 200 Mbps $2^{15}$-1 PRBS input.

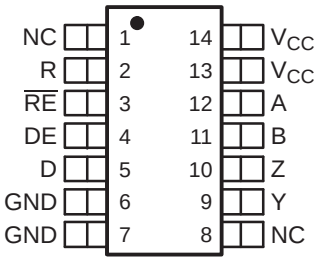
**Figure 12. Receiver Jitter Measurement Waveforms**

## PIN ASSIGNMENTS

**SN65MLVD201D (Marked as MF201)**
**SN65MLVD206D (Marked as MF206)**
**(TOP VIEW)**




**SN65MLVD203D (Marked as MLVD203)**
**SN65MLVD207D (Marked as MLVD207)**
**(TOP VIEW)**




NC - No internal connection

## DEVICE FUNCTION TABLES

**TYPE-1 RECEIVER (201, 203)**

| INPUTS | | OUTPUT |
|---|---|---|
| $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R |
| $V_{ID} \geq 50$ mV | L | H |
| $-50$ mV $< V_{ID} < 50$ mV | L | ? |
| $V_{ID} \leq -50$ mV | L | L |
| X | H | Z |
| X | Open | Z |
| Open Circuit | L | ? |

**TYPE-2 RECEIVER (206, 207)**

| INPUTS | | OUTPUT |
|---|---|---|
| $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R |
| $V_{ID} \geq 150$ mV | L | H |
| 50 mV $< V_{ID} < 150$ mV | L | ? |
| $V_{ID} \leq 50$ mV | L | L |
| X | H | Z |
| X | Open | Z |
| Open Circuit | L | L |

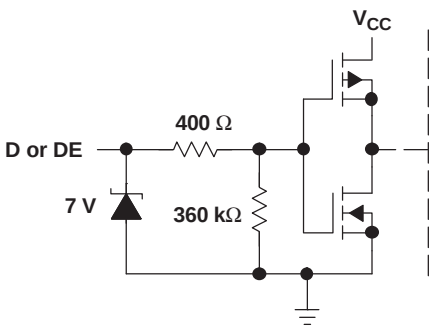
**DRIVER**

| INPUT | ENABLE | OUTPUTS | |
|---|---|---|---|
| D | DE | A OR Y | B OR Z |
| L | H | L | H |
| H | H | H | L |
| OPEN | H | L | H |
| X | OPEN | Z | Z |
| X | L | Z | Z |

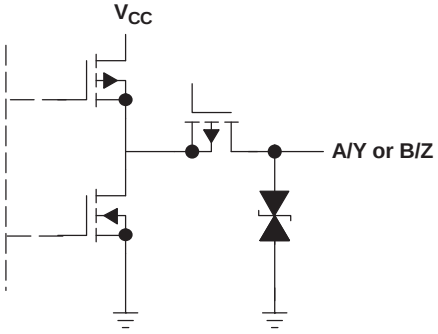
H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

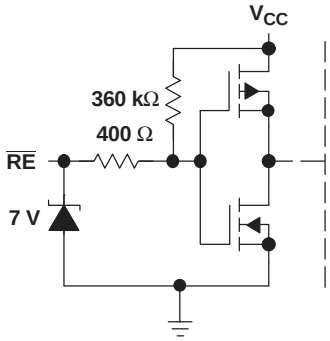
**DRIVER INPUT AND DRIVER ENABLE**



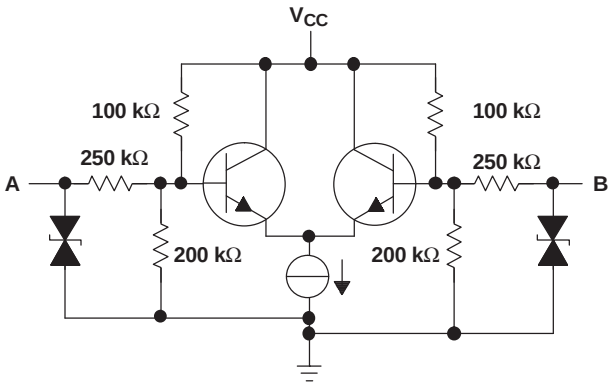

**DRIVER OUTPUT**



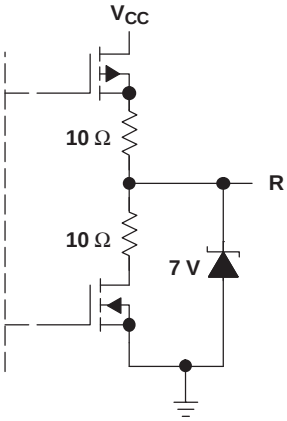

**RECEIVER ENABLE**




**RECEIVER INPUT**




**RECEIVER OUTPUT**



## TYPICAL CHARACTERISTICS

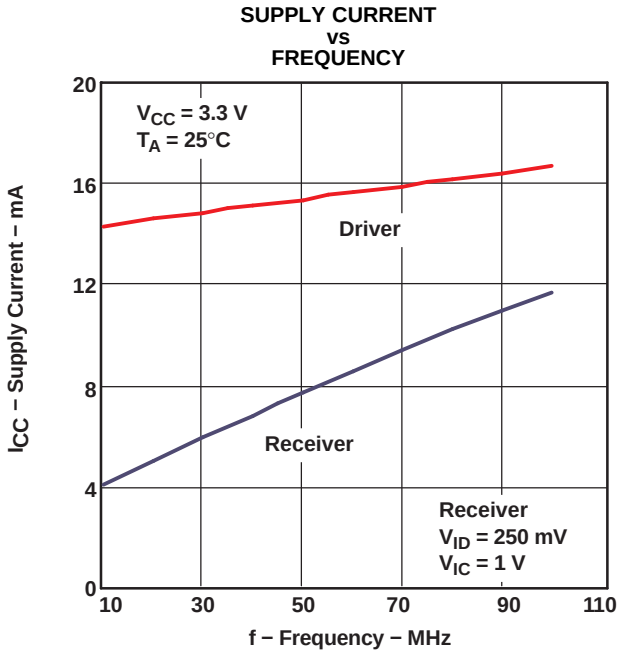



Figure 13.

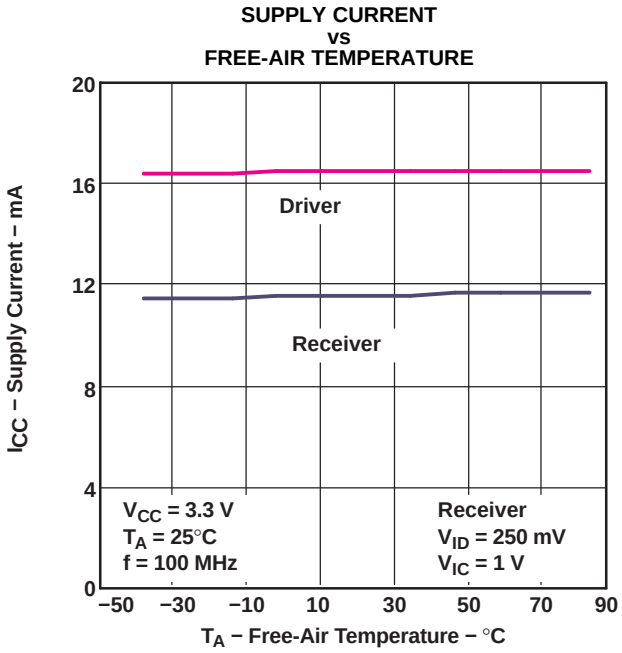



Figure 14.

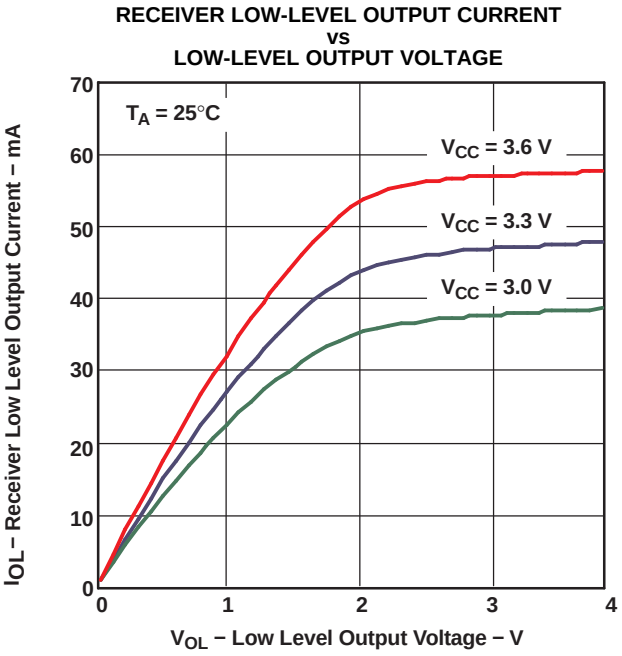



Figure 15.

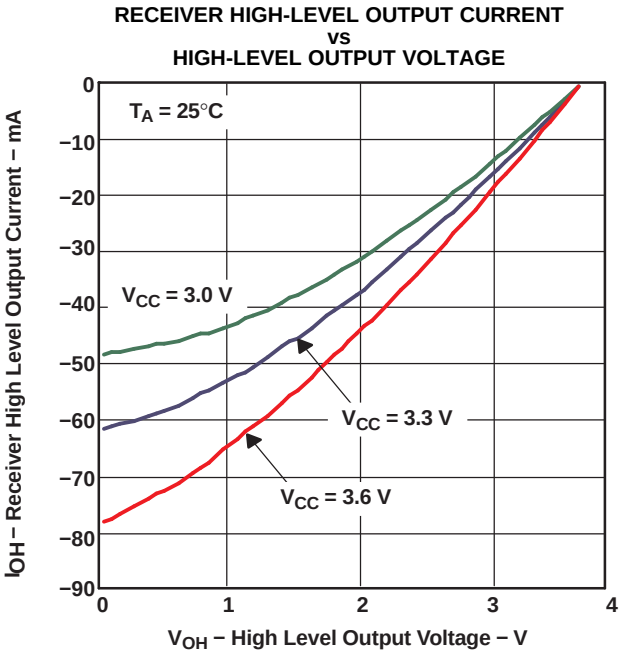



Figure 16.

## TYPICAL CHARACTERISTICS (continued)

**DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT**

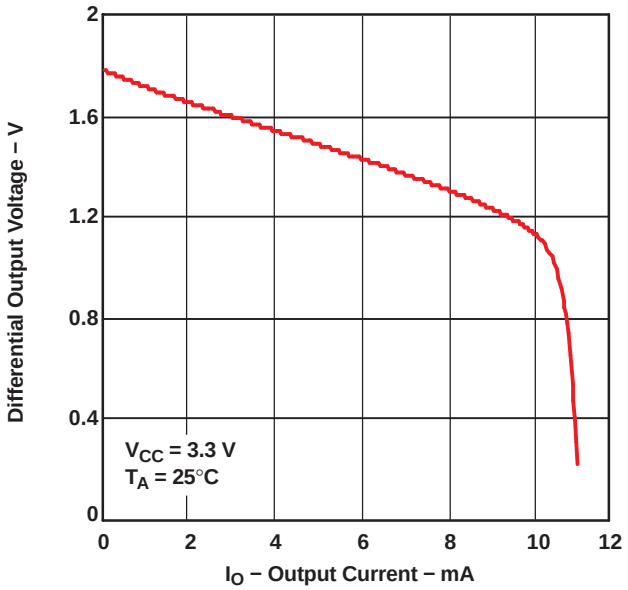



Figure 17.

**DRIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE**

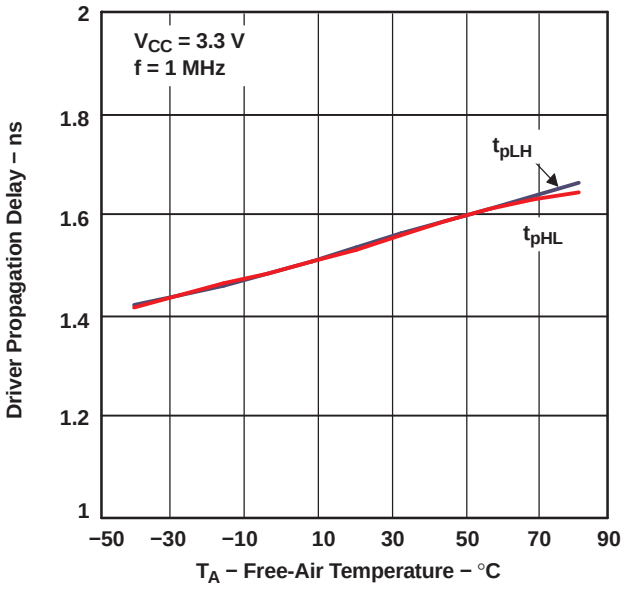



Figure 18.

**RECEIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE**

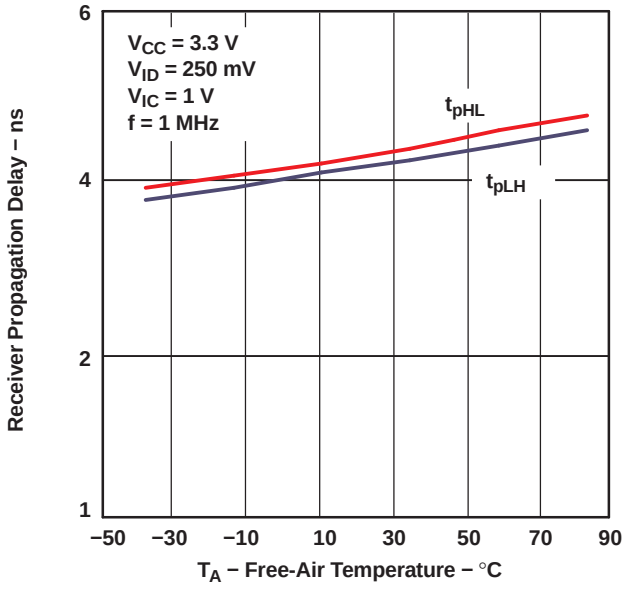



Figure 19.

**ADDED DRIVER CYCLE-TO-CYCLE JITTER (PEAK) vs FREQUENCY**

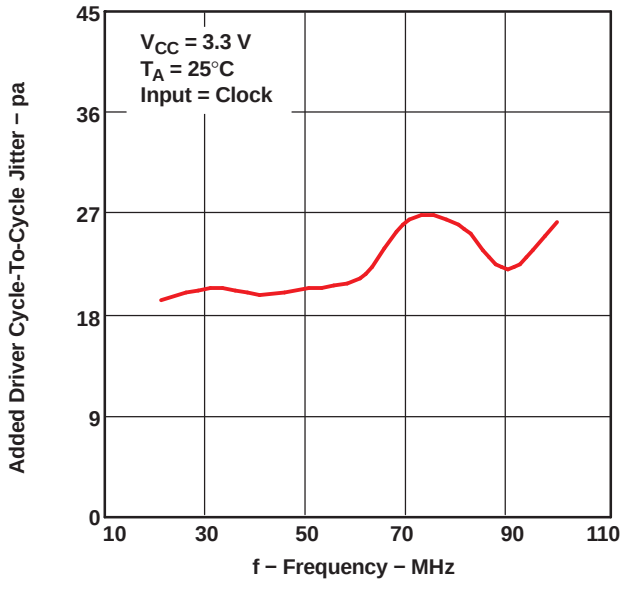



Figure 20.

## TYPICAL CHARACTERISTICS (continued)

**ADDED DRIVER PEAK-TO-PEAK JITTER vs DATA RATE**

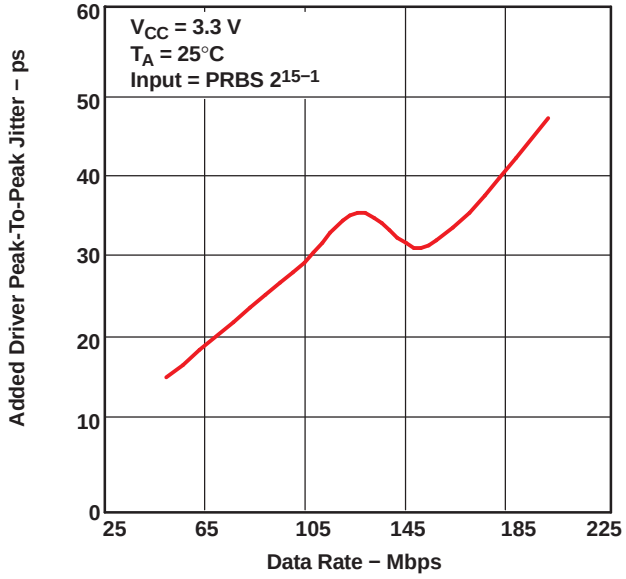



Figure 21.

**ADDED DRIVER PEAK-TO-PEAK JITTER vs FREE-AIR TEMPERATURE**

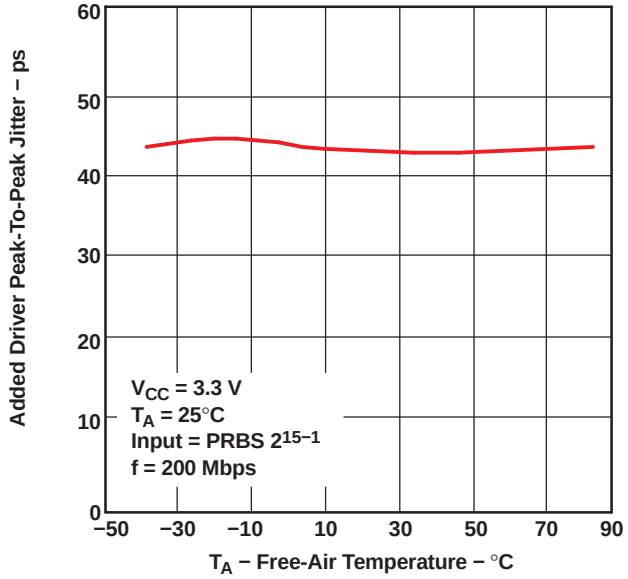



Figure 22.

**ADDED RECEIVER CYCLE-TO-CYCLE JITTER vs FREQUENCY**

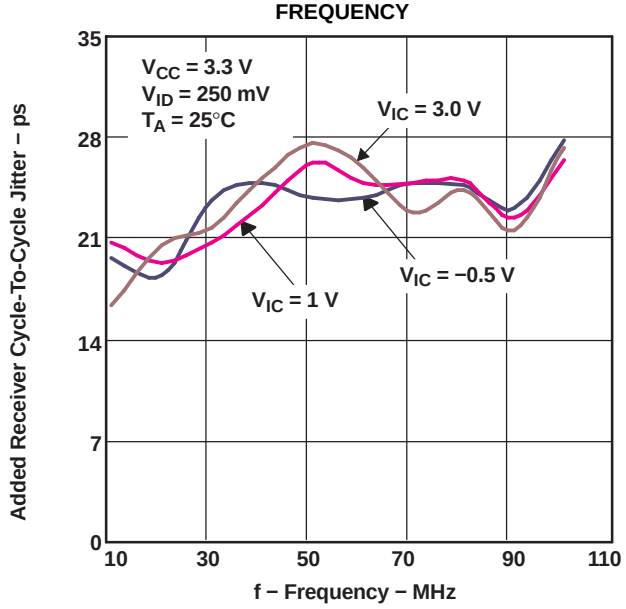



Figure 23.

**ADDED RERCEIVER PEAK-TO-PEAK JITTER vs FREE-AIR TEMPERATURE**

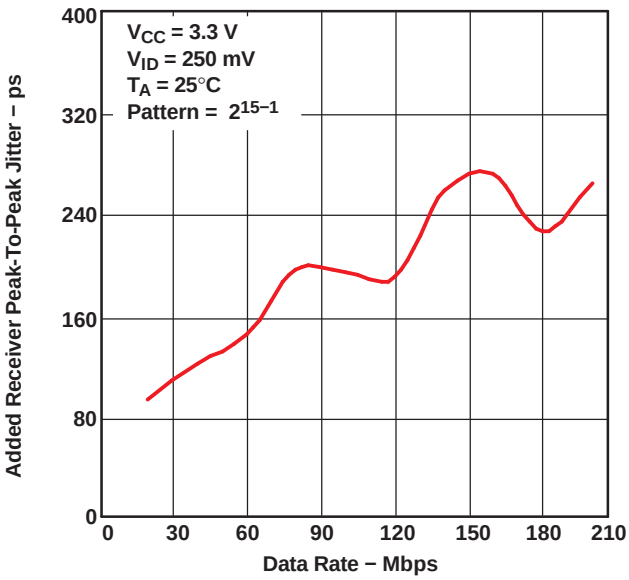



Figure 24.

## TYPICAL CHARACTERISTICS (continued)

**ADDED RECEIVER PEAK-TO-PEAK JITTER vs FREE-AIR TEMPERATURE**

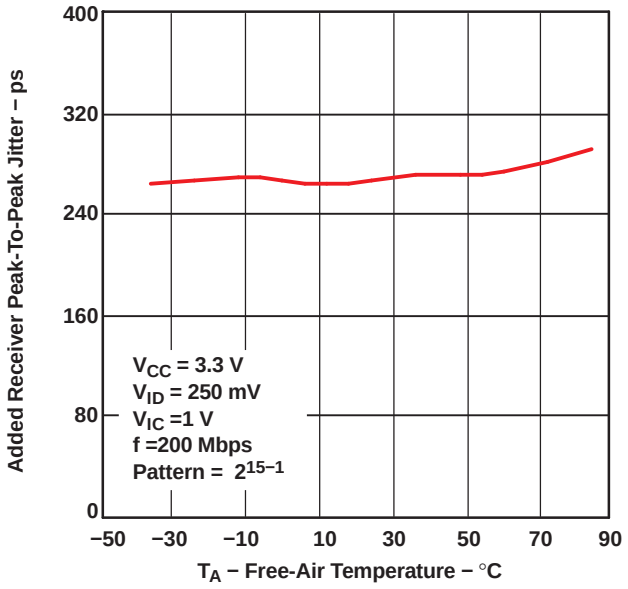
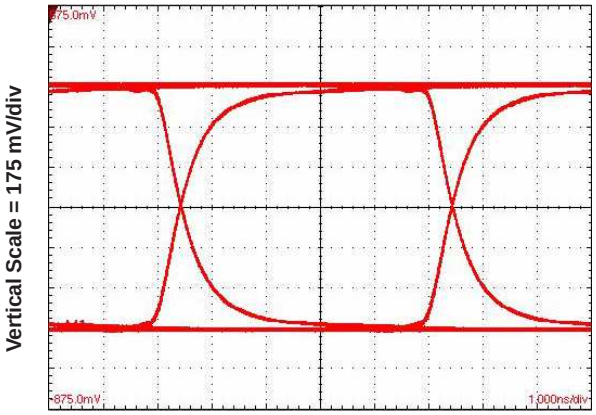



**Figure 25.**

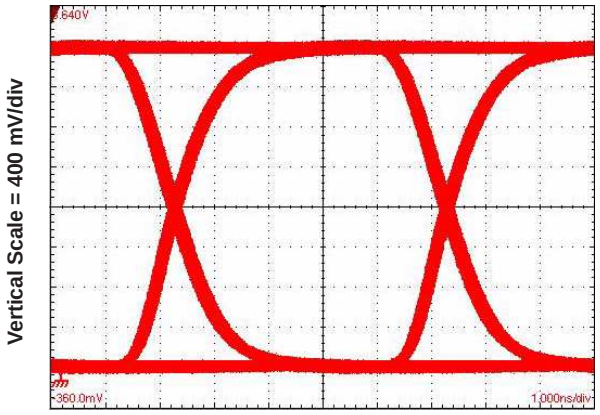
**SN65MLVD201 DRIVER OUTPUT EYE PATTERN**
**200 Mbps, $2^{15-1}$ PRBS, $R_L$ = 50 Ω**




**Horizontal Scale = 1 ns/div**

**Figure 26.**

**SN65MLVD201 RECEIVER OUTPUT EYE PATTERN**
**200 Mbps, $2^{15-1}$ PRBS, $R_L$ = 15 Ω**




**Horizontal Scale = 1 ns/div**

**Figure 27.**

## APPLICATION INFORMATION

### Receiver Input Threshold (Failsafe)

The MLVD standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 3 and Figure 28.

**Table 3. Receiver Input Voltage Threshold Requirements**

| RECEIVER TYPE | OUTPUT LOW | OUTPUT HIGH |
|---|---|---|
| Type 1 | $-2.4\ V \le V_{ID} \le -0.05\ V$ | $0.05\ V \le V_{ID} \le 2.4\ V$ |
| Type 2 | $-2.4\ V \le V_{ID} \le 0.05\ V$ | $0.15\ V \le V_{ID} \le 2.4\ V$ |

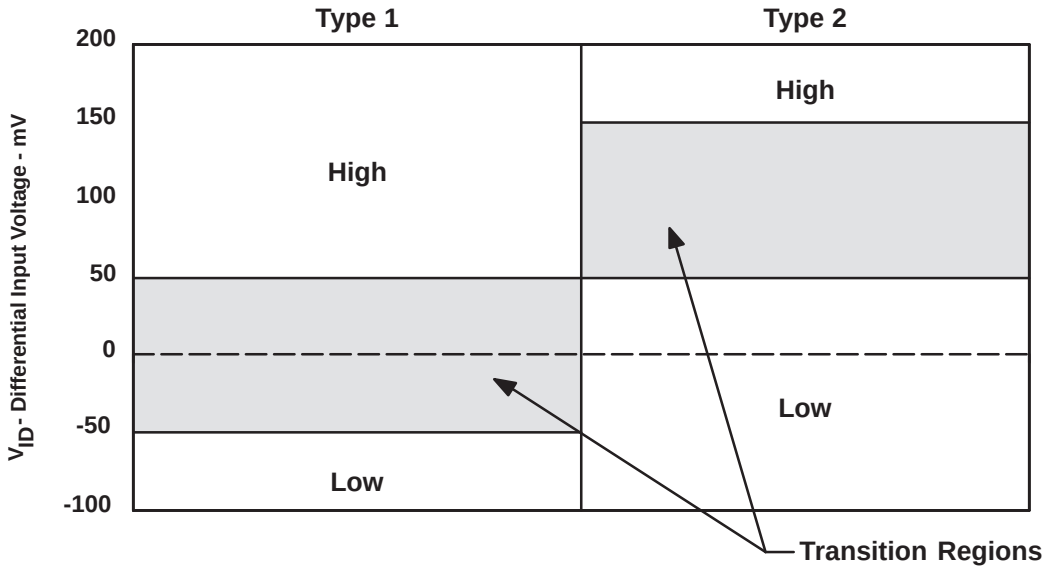



**Figure 28. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region**

## LIVE INSERTION/GLITCH-FREE POWER UP/DOWN

The SN65MLVD201/203/206/207 family of products offered by Texas Instruments provides a glitch-free powerup/down feature that prevents the M-LVDS outputs of the device from turning on during a powerup or powerdown event. This is especially important in live insertion applications, when a device is physically connected to an M-LVDS multipoint bus and VCC is ramping.

While the M-LVDS interface for these devices is glitch free on powerup/down, the receiver output structure is not.Figure 29 shows the performance of the receiver output pin, R (CHANNEL 2), as Vcc (CHANNEL 1) is ramped.

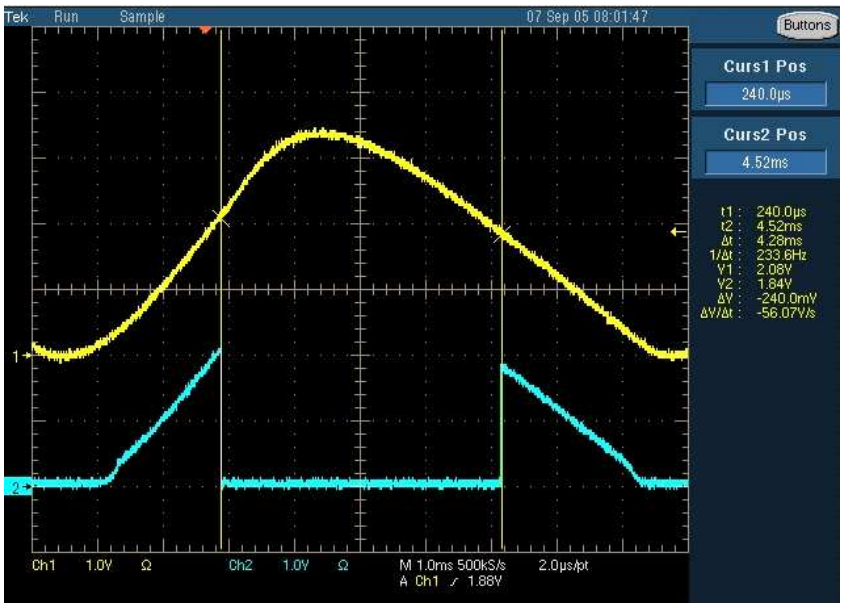



**Figure 29. M-LVDS Receiver Output: VCC (CHANNEL 1), R Pin (CHANNEL 2)**

The glitch on the R pin is independent of the $\overline{RE}$ voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until VCC has reached a steady state value.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN65MLVD201D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD201DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD201DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD201DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD203D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD203DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD203DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD203DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD206D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD206DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD206DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD206DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD207D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD207DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD207DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65MLVD207DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

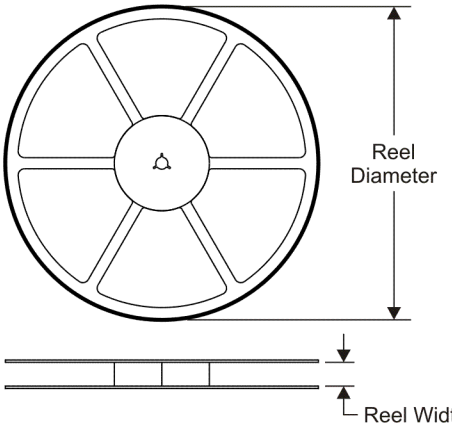
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

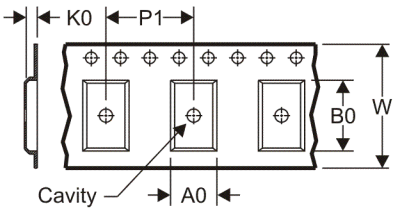
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

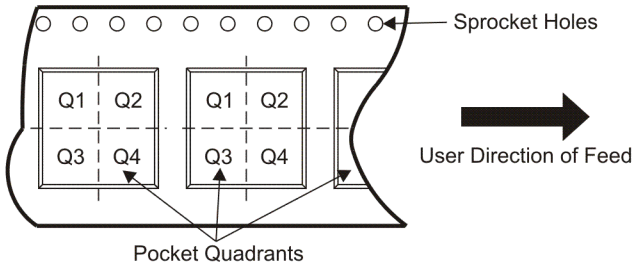



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

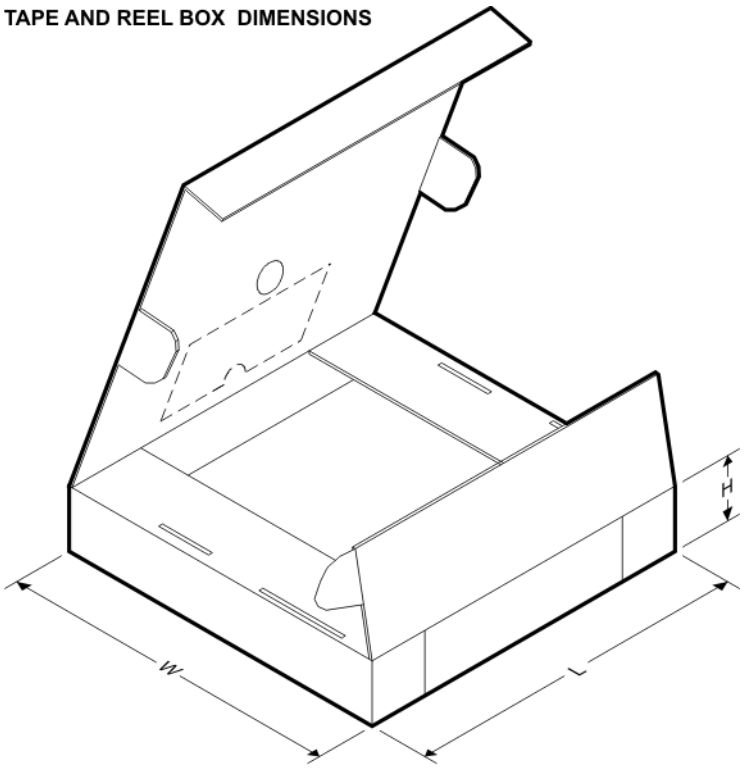
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65MLVD201DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65MLVD203DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65MLVD206DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65MLVD207DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

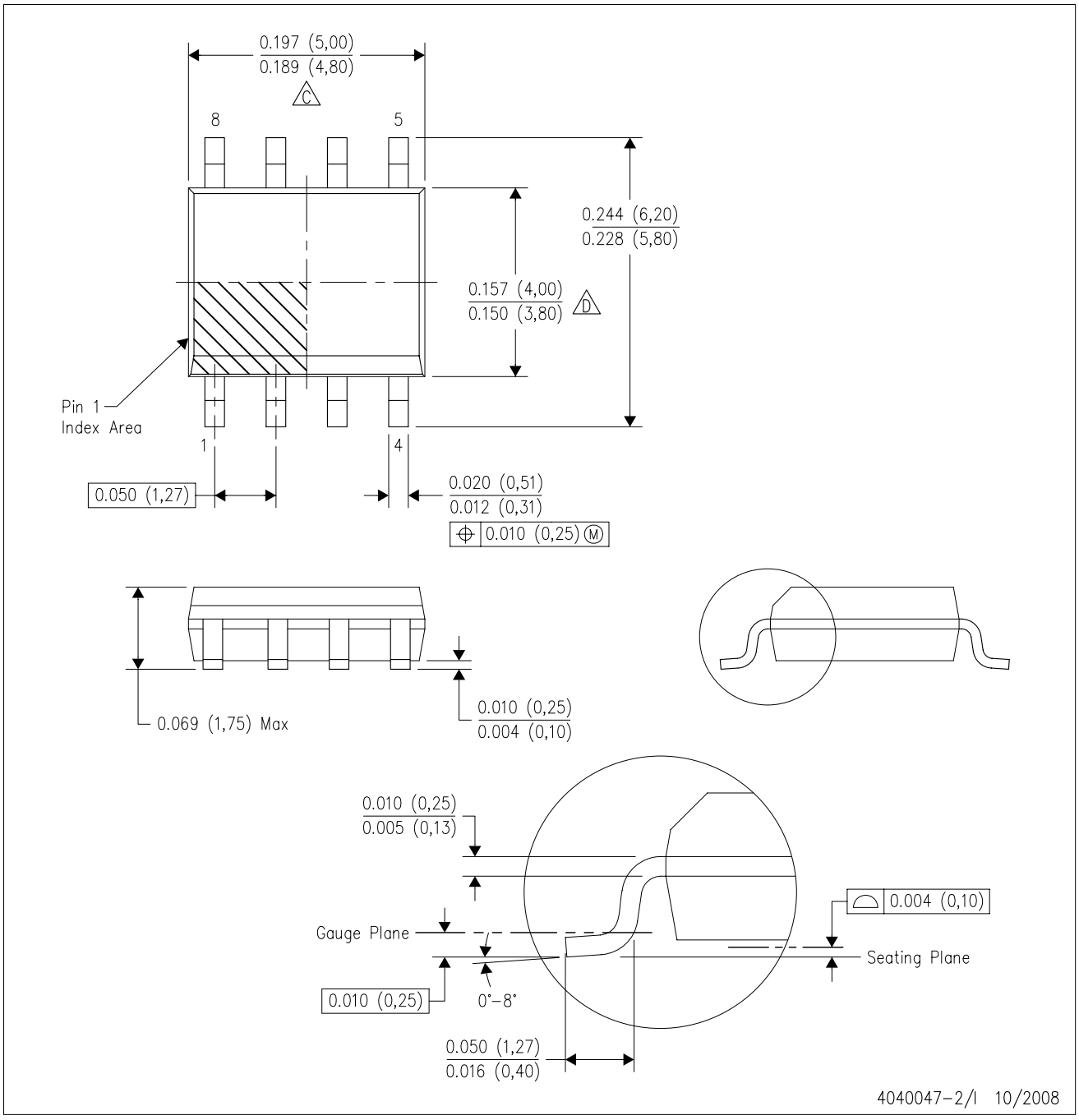
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

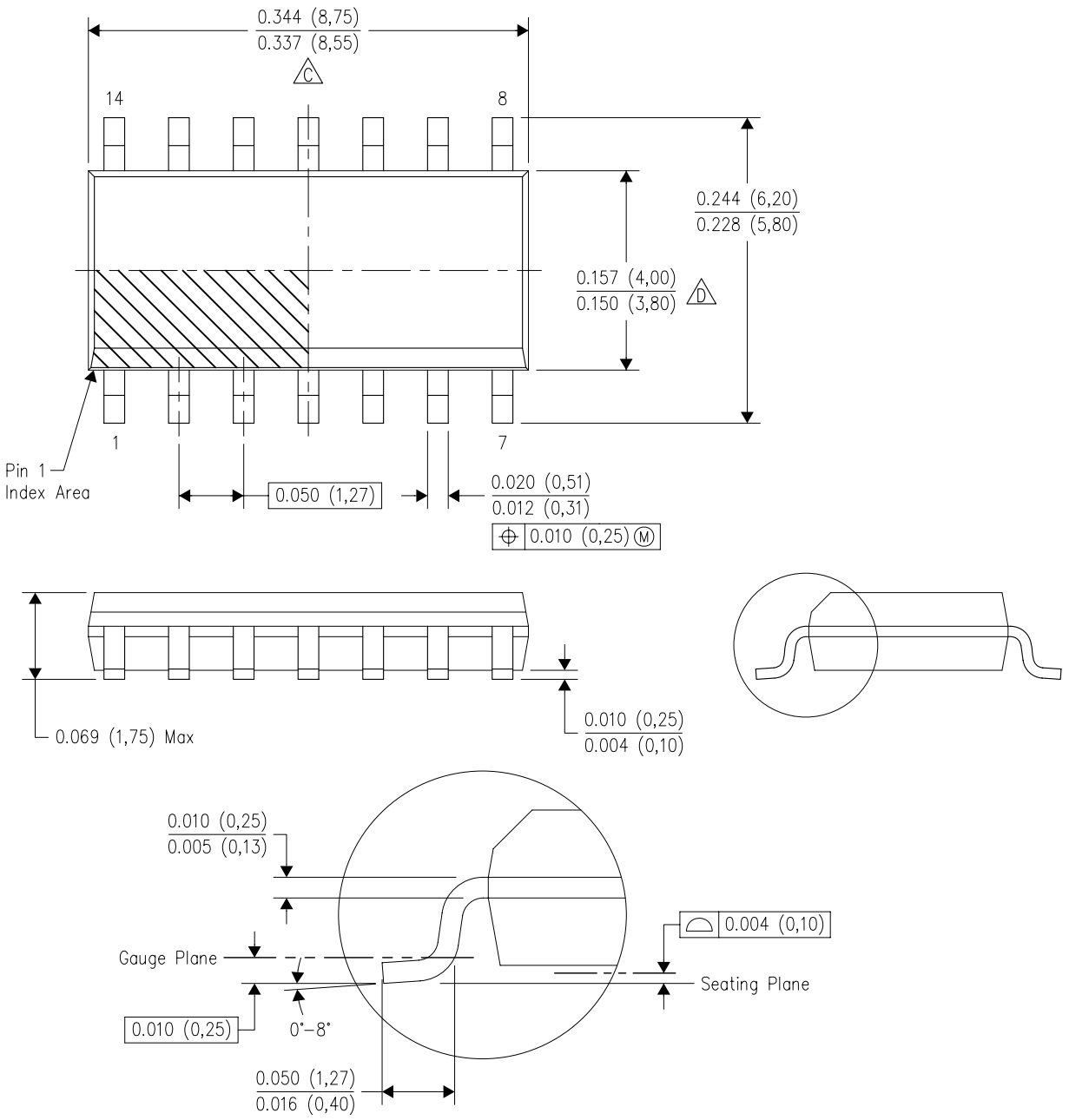
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65MLVD201DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65MLVD203DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN65MLVD206DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65MLVD207DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

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